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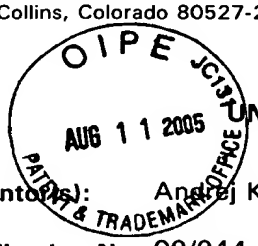
PATENT APPLICATION

ATTORNEY DOCKET NO. 200301967-2



IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Andrej Kocev et al.

Confirmation No.: 1813

Application No.: 09/944,776

Examiner: Pham, Thomas K.

Filing Date: 08/31/01

Group Art Unit: 2121

Title: PROGRAMMABLE TUNING FOR FLOW CONTROL AND SUPPORT FOR CPU HOT PLUG

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on **June 10, 2005**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$120.00
( )	two months	$450.00
( )	three months	$1020.00
( )	four months	$1590.00

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( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$500.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

(X) I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450. Date of Deposit: **August 9, 2005**

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Number of pages: **22**

Typed Name: **Melissa L. Altman**

Signature: Melissa Altman

Respectfully submitted,

Andrej Kocev et al.

By _____

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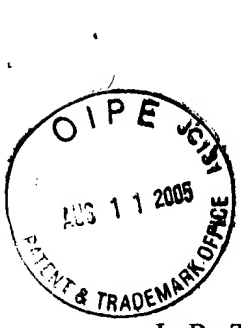

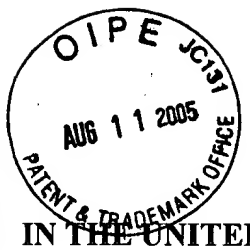

PATENTS
15311-2310

AFV

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re The Application of:
Andrej Kocev et al.

Serial No.: 09/944,776

Filed: August 31, 2001

For: Programmable Tuning for Flow Control and Support for CPU Hot Plug

Examiner: Pham, Thomas K.

Art Unit: 2121

Cesari and McKenna, LLP
88 Black Falcon Avenue
Boston, MA 02210
August 9, 2005

CERTIFICATE OF MAILING

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Melissa L. Altman

X Appeal Brief
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X Transmittal of Appeal Brief

PATENTS
15311-2310
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Melissa Altman
Melissa Altman

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

APPEAL BRIEF

In response to the Notice of Appeal mailed June 10, 2005, Applicants hereby submit this Appeal Brief.

REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, L.P. of Houston, Texas.

RELATED APPEALS AND INTERFERENCES

Applicants and their legal representatives know of no related appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in the present appeal.

STATUS OF CLAIMS

Claims 1-12 have been canceled. Claims 13-41 are pending in the case. Claims 13-41 stand finally rejected under 35 U.S.C. §103.

A copy of claims 13-41, in their current form, is attached hereto as an Appendix.

STATUS OF AMENDMENTS

No amendments have been filed since the mailing of the Final Rejection on March 30, 2005.

SUMMARY OF CLAIMED SUBJECT MATTER

The summary is set forth in four exemplary embodiments that correspond to independent claims 13, 15, 21 and 32. Discussions about elements and recitations of these claims can be found at least at the cited locations in the specification and drawings.

Independent Claim 13 is directed to a method for programmatically allocating system resources to accommodate input/output (I/O) transactions at I/O ports of a multiprocessor computer. The claimed method includes determining the number of devices being serviced by the I/O ports (see pp. 3 and 9-10), identifying an assembly for hot

swapping (see p. 11), copying the contents of cache memories associated with the assembly to be hot swapped (see pp. 3 and 12-13), setting criteria for transactions at the I/O ports with regard to the number of devices determined to be serviced thereby (see p. 10), and assigning resources to the I/O ports with respect to the number of devices determined to be serviced thereby (see p. 10).

Independent claim 15 is directed to a system for allocating resources to accommodate I/O transactions at the I/O ports of a multiprocessor computer. The system includes means for determining the number of devices being serviced by the I/O ports (see pp. 3 and 9-10, and Figs. 7-8), an assembly for hot swapping (see pp. 5-6 and 11, and Fig. 3), means for copying the contents of cache memories associated with the assembly to be hot swapped (see pp. 3 and 13-13, and Figs. 7-8), means for setting criteria for transactions at the I/O ports with regard to the number of devices determined to be serviced thereby (see p. 10 and Figs. 7, 8 and 10B), and means for assigning resources to the I/O ports, whereby the assigning means are responsive to the criteria (see p. 10 and Figs. 7, 8 and 10B).

Independent claim 21 is directed to a method for programmatically allocating resources for processing I/O transactions at the I/O ports of an I/O bridge. The claimed method includes identifying the number of I/O devices being serviced by an I/O port (see pp. 3 and 9-10), setting criteria for the transactions at the I/O port based upon the number of devices that it services (see p. 10), and assigning resources to the I/O port in response to the criteria that have been set (see p. 10).

Independent claim 32 is directed to an I/O bridge for use in a multiprocessor computer. The I/O bridge includes a plurality of I/O ports for communicating with I/O devices that generate or receive transactions (see p. 6, and Figs. 4 and 7), resources for use in servicing those transactions (see pp. 9-10, and Fig. 8), and programmable logic that assigns the resources among the I/O ports in response to the number of I/O devices to which the I/O ports are communicating (see pp. 10-12, and Figs. 10-12).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 13-17, 19, 21 and 31, which otherwise meet all conditions of patentability under Title 35 of the United States Code, are unpatentable under 35 U.S.C. §103 over U.S. Patent No. 5,864,679 to Kanai et al. ("Kanai") in view of U.S. Pat. No. 6,718,413 to Wilson ("Wilson") and U.S. Patent No. 6,219,734 to Wallach et al. ("Wallach"), where the art of record either alone or in combination fails to teach or suggest, among other things, setting criteria for transactions at a port with regard to the number of devices serviced by the port, or assigning resources to the port based on the number of devices being serviced.

Whether claim 32, which otherwise meets all conditions of patentability under Title 35 of the United States Code, is unpatentable under §103 over Wallach in view of U.S. Pat. No. 6,119,185 to Westerinen et al. ("Westerinen"), where the art of record either alone or in combination fails to teach or suggest, among other things, programmable logic that assigns resources among input/output (I/O) ports in response to the number of I/O devices with which the I/O ports are communicating.

ARGUMENT

Independent Claims 13, 15 and 21

Applicants respectfully submit that, in rejecting independent claims 13, 15 and 21, the final Office Action ignores certain, positively recited language appearing in the claims, and fails to identify any prior art reference that purportedly teaches or suggests this ignored claim language.

More specifically, independent claim 13 recites, in relevant part, as follows:

> "A method for programmably allocating resources to accommodate I/O transactions at I/O ports of a multiprocessor computer system comprising:"
>
> "determining the number of devices being serviced via the ports",
>
> "setting criteria **for transactions** at the port **with respect to the number of devices**", and
>
> "with respect to the numbers of devices at the ports, assigning resources to the ports".

In other words, claim 13 recites that criteria are set for transactions at the port with respect to the number of devices being serviced by the port, and resources are assigned to the ports based on the number of devices being serviced thereby.

The final Office Action, at p. 3, cites to Col. 5, lines 41-43 of Kanai as purportedly teaching "setting parameters [criteria] for routing transactions to the port", and to Col. 6, lines 10-19 of Wilson as purportedly teaching "assigning devices [resources] to the ports". Neither of these references, however, provide any teaching or suggestion either for the setting of criteria "with respect to the number of devices" being serviced by the ports, or for assigning resources to the ports "with respect to the numbers of devices at the ports".

A review of Kanai reveals that what it teaches is to (1) **extract** certain features from a given transaction, and then, based on the extracted features, (2) route the given transaction to a particular processor for processing. This is also confirmed in the excerpt of Kanai that is cited in the final Office Action (i.e., Col. 5, lines 41-43), which states:

> means for routing each transaction to one of the transaction processors according to the feature parameters **extracted** by the extracting means and the processing history information stored by the storing means.

As shown, there is no teaching or suggestion from this excerpt of Kanai for the setting of any criteria. Nor is there any teaching or suggest for the setting of criteria for transactions at the ports with respect to the numbers of devices being serviced by the ports. Instead, what Kanai is describing here is the forwarding of transactions, such as a bank withdrawal transaction, to specific processors according to particular parameters that are found within the transactions themselves. Kanai, Col. 15, lines 33-45 and Fig. 10.

The second excerpt of Kanai relied upon in the final Office Action also fails to provide any teaching or suggestion for "setting criteria for transactions at the port with respect to the number of devices". At p. 13, the final Office Action cites to Col. 23, lines 14-28. In this excerpt, Kanai mentions that his transaction processing system can be configured so that the transactions arriving at more than one port can all be received at the same transaction reception unit 103. In other words, what Kanai is suggesting is that his transaction processing system can be wired-up such that the transactions from more than one port all go to the same transaction reception unit 103. See Figs. 25 and 26, which show multiple transaction sources (items 102) being wired to the same transaction reception unit (item 103).

However, as noted above, claim 13 recites "setting criteria for transactions at the port with respect to the number of devices". This second excerpt from Kanai provides no teaching or suggestion for the setting of any criteria, nor does it provide any teaching or suggestion for setting criteria for transaction at the port **with respect to the number of devices** at the port. Thus, this new excerpt of Kanai also fails to teach or suggest the present invention.

In fact, Kanai actually teaches away from the present invention. That is, rather than setting criteria for transactions at a port, Kanai examines each transaction and makes a decision where to send that transaction for processing, based on parameters extracted from the transaction itself. Thus, Kanai teaches a system that operates on a transaction-by-transaction basis such that each transaction is separately considered. To the contrary, claim 13 recites setting criteria for transactions **at a port** with respect to the number of devices.

Wilson too fails to teach or suggest the limitations of claims 13-31. Basically, Wilson is directed to a system for reducing the number of interrupts generated when a plurality of devices all contend for access to a bus in order to transfer data to a processor. The particular excerpt of Wilson (col. 6, lines 10-19) cited in the final Office Action states as follows:

> The host adapter circuitry 316 is coupled to one or more SCSI devices 306 by means of the SCSI bus 308. It should be noted that the computer system 300 may include any suitable number of SCSI devices depending on the type of SCSI bus implemented. Each of the SCSI devices is preferably assigned a unique ID that indicates its priority among the SCSI devices. The SCSI devices 306 may include, but not limited to, devices such as disk drives, tape drives, printers, scanners, optical drives, or any other devices that meet the SCSI specifications.

As shown, there is no mention in this excerpt of the assigning of any resources to **ports**. Furthermore, there is no teaching or suggestion of assigning resources to ports based on the numbers of devices that the ports are servicing. Instead, this excerpt merely states that SCSI devices may be assigned unique IDs, which can then be used to indicate priority among them.

Because the final Office Action fails to cite any reference for teaching or suggesting the invention, **as claimed**, the rejection of claim 13 should be reversed. See MPEP §2143.03 (All of the claim's limitations must be taught or suggested by the prior art to support a prima facie §103 rejection.)

For these reasons, among others, the rejection of independent claim 13 should be reversed.

Independent claim 15, in relevant part, recites as follows:

> "means for setting criteria for transactions **at the port** with respect to the number of devices".

Likewise, independent claim 21, in relevant part, recites as follows:

> "setting criteria for the transactions at the **at least one I/O port** with respect to the number of I/O devices being serviced by the port".

For the reasons set forth above in connection with claim 13, the art of record fails to teach or suggest Applicants' claimed "means for setting criteria for transactions **at the port** with respect to the number of devices" as recited in claim 15, or the claimed "setting criteria for the transactions **at the least one I/O port** with respect to the number of I/O devices being serviced by the port" as recited in claim 21. Therefore, the rejection of independent claims 15 and 21 should be reversed.

Dependent claims 14, 16 and 31

In the final Office Action, claims 14, 16 and 31 were rejected as obvious based on Wallach. Specifically, the final Office Action cites to at Col. 10, lines 58-61 of Wallach. Applicants respectfully disagree that Wallach teaches or suggests the invention set forth in these dependent claims.

Claim 14, which depends from claim 13, recites as follows:

> "wherein assigning resources to the ports comprises at least one of assigning control registers to the ports, assigning direct memory access engines to the ports, assigning cache memory to the ports and assigning priorities among the transactions at the ports."

The excerpt from Wallach on which the final Office Action relies as purportedly teaching or suggesting this limitation reads as follows:

> "Once an adapter 310 is added to the computer system, system resources must be allocated for the adapter 310. The configuration manager 500 then configures the newly added adapter 310 (state 604) by writing information to the adapter's configuration space registers."

As shown, this excerpt discloses that, when a new adapter is added to Wallach's computer system, a configuration manager configures the new adapter for operation by writing certain information to the adapter's registers. Applicants respectfully submit that this excerpt provides no teaching or suggestion for the assignment of registers (as a resource) to the I/O ports of a multiprocessor computer system. Indeed, there is no mention by Wallach of somehow assigning registers or any other resource to the ports. Instead, the excerpt simply provides that information must be written to the new adapter's registers in order to configure it. Because Wallach fails to teach or suggest the "assigning of control registers **to the ports**", the rejection of claim 14 should be reversed.

Claim 16 depends from claim 15 and is similar to claim 14. Accordingly, for the reasons set forth above with regard to claim 14, among others, the rejection of claim 16 should also be reversed.

Claim 31, which depends from claim 21, recites as follows:

> "the I/O bridge comprises at least one control register, the at least one control register having a plurality of fields, and at least one field of the control register being associated with a corresponding resource, and"
>
> "the method further comprising **writing to a selected field** of the at least one control register **so as to modify the assignment of resources.**"

As shown above, the Wallach excerpt, on which the final Office Action relies for rejecting claim 31, provides no teaching or suggestion for writing to a selected field of a control register of an I/O bridge in order to modify the assignment of resources to an I/O port. Instead, at most, Wallach discloses that its adapter has registers which can be written to so as to configure the adapter. Again, there is no teaching or suggestion in this excerpt for providing a field of a register which can be written to in order to modify the assignment of resources to an I/O port. Because the cited excerpt of Wallach fails to teach or suggest the limitation of claim 31, the rejection should be reversed.

Dependent claims 17 and 19

In the final Office Action, claims 17 and 19 were rejected as obvious based on Kanai. Applicants respectfully submit that the art of record, including Kanai, fails to teach or suggest the invention of claims 17 and 19.

Claim 17, in relevant part, recites:

> "determining the number and types **of transactions anticipated at the ports,** wherein the assignment of resources is further with respect to the numbers and types of transactions at the ports".

The excerpt from Kanai on which the final Office Action relies, states as follows:

> "A position of the type of transaction in the packet of the RPC is fixed, so that the transaction reception unit 103 which received the packet can extract the type of transaction from the received packet, and the transaction reception unit 103 supplies the extracted type of transaction to the transaction table 126. Here, it is also possible to provide a configuration in which the transaction reception unit 103 can receive the transaction packet arriving at a plurality of ports. In such a case, it is also possible to produce the transaction table for recording the information concerning the transactions arrived at that port for each port, such that when the packet is received, the transaction reception unit 103 supplies the type of transmission to the transaction table corresponding to the port from which this transaction has been received.

In other words, what Kanai is describing here is that transaction packets include a type field (see Fig. 10 "transaction type"), and this field can be examined by Kanai's transaction reception unit 103. Applicants submit that this excerpt of Kanai fails to teach or suggest the assignment of resources to ports based on the numbers and types of transactions anticipated at the ports. Accordingly, the rejection of claim 17 based on Kanai should be reversed.

Claim 19, which depends from claim 15, is similar to claim 17, and was also rejected based on this same excerpt of Kanai. For the reasons set forth above, among others, the rejection of claim 19 should also be reversed.

Independent claim 32

Applicants respectfully submit that the art of record fails to teach or suggest the invention of independent claim 32. This claim, in its entirety, recites as follows:

> "An Input/Output (I/O) bridge for use in a computer system having a plurality of processors, the I/O bridge comprising:"
>
> "a plurality of I/O ports, each I/O port configured to communicate with at least one I/O device that generates or receives transactions;"

> "resources for use in servicing the transactions of the I/O devices; and"
>
> "programmable logic configured and arranged to assign the resources **among the I/O ports** in response to the number of I/O devices with which the I/O ports are communicating."

As shown, claim 32, among other things, recites programmable logic disposed at an I/O bridge that is configured "to assign the resources **among the I/O ports**" on the basis of the number of I/O devices that are communicating with the I/O ports.

The final Office Action, at p. 8, cites to Col. 2, lines 1-12 of Westerinen as teaching Applicants' claimed "programmable logic" limitation. Applicants respectfully disagree that Westerinen teaches or suggests the assigning of resources among the I/O ports "in response to the number of I/O devices with which the I/O ports are communicating". Indeed, Westerinen provides no teaching or suggestion for determining the number of I/O devices to which various ones of the ports are communicating. Westerinen similarly fails to teach or suggest the assignment of resources among I/O ports in response to that information.

Westerinen is basically directed to configuring a computer system. The cited excerpt of Westerinen (col. 2, lines 1-12), moreover, states as follows:

> processing logic that performs control and data processing functions; a plurality of resources that have resource settings therefore that are coupled to said processing logic and including at least interrupts and memory; a plurality of devices which require access to one or more of said plurality of resources; and **configuration logic that assigns**, substantially in parallel, **two or more of said plurality of devices to said resources**. Another embodiment of the present invention includes similar features and configuration logic that decides the order in which two or more of said plurality of devices are assigned to one of said plurality of resources before making an assignment of those two of more devices to that resource.

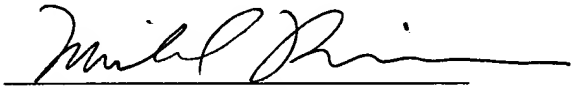
As shown, Westerinen discloses configuration logic that assigns devices directly to resources. This is not, however, what claim 32 recites. Claim 32 recites programmable logic configured to assign resources **among I/O ports** to which the devices, in turn, may be coupled.

Thus, what Westerinen teaches is the assignment **of devices** directly to the resources, so that each device is assigned to a particular resource. There is no teaching or suggestion by Westerinen to assign resources **among I/O ports**. Instead, Westerinen operates solely at the device level, and provides no teaching or suggestion for assigning resources among I/O ports. Because Westerinen fails to teach or suggest logic assigning resources among I/O ports, the rejection of claim 32 should be reversed.

CONCLUSION

Applicants respectfully submit that the claims are allowable over the art of record. Accordingly, Applicants request that the rejection of all claims be reversed.

Respectfully submitted,



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CLAIMS APPENDIX
(Claims on Appeal in Appl. Ser. No. 09/944,776)

Claims 1-12 (Canceled)

13. (Previously presented) A method for programmably allocating resources to accommodate I/O transactions at I/O ports of a multiprocessor computer system comprising:

determining the number of devices being serviced via the ports,

identifying at least one assembly for hot swapping,

copying the contents of cache memories associated with the at least one identified assembly,

setting criteria for transactions at the port with respect to the number of devices, and

with respect to the numbers of devices at the ports, assigning resources to the ports.

14. (Previously presented) The method as defined in claim 13 wherein assigning resources to the ports comprises at least one of assigning control registers to the ports, assigning direct memory access engines to the ports, assigning cache memory to the ports and assigning priorities among the transactions at the ports.

15. (Previously presented) A system for programmably allocating resources to accommodate I/O transactions at I/O ports of a multiprocessor computer system, the system comprising:

means for determining the number of devices being serviced via a port,

at least one assembly identified for hot swapping,

means for copying the contents of cache memories associated with the at least one identified assembly,

means for setting criteria for transactions at the port with respect to the number of devices, and

means, responsive to the criteria, for assigning resources to the ports.

16. (Previously presented) The system as defined in claim 15 wherein the resources assigned to the ports comprises at least one of

direct memory access (DMA) engines,

cache memory, and

means for assigning priorities among the transactions at the ports.

17 (Previously presented) The method as defined in claim 13 further comprising determining the number and types of transactions anticipated at the ports, wherein the assignment of resources is further with respect to the numbers and types of transactions at the ports.

18. (Previously presented) The method as defined in claim 13 wherein the at least one identified assembly has a memory system, and the method further comprises copying the states and status of the memory systems associated with at least one identified assembly.

19. (Previously presented) The system as defined in claim 15 further comprising means for determining the number and types of transactions anticipated at the ports, wherein the criteria further accounts for the anticipated number and types of transactions.

20. (Previously presented) The system as defined in claim 15 wherein the at least one identified assembly has a memory system, and the system further comprises means for copying the states and status of the memory systems associated with the at least one identified assembly.

21. (Previously presented) A method for programmably allocating resources for processing Input/Output (I/O) transactions at a plurality of I/O ports of an I/O bridge, the method comprising:

identifying the number of I/O devices being serviced by at least one I/O port;

setting criteria for the transactions at the at least one I/O port with respect to the number of I/O devices being serviced by the port; and

assigning the resources to the at least one I/O port in response to the criteria.

22. (Previously presented) The method of claim 21 wherein the assigning comprises assigning a plurality of direct memory access (DMA) engines for use in processing I/O transactions.

23. (Previously presented) The method of claim 22 wherein assigning comprises apportioning a selected number of DMA engines to process a given transaction at a particular I/O port.

24. (Previously presented) The method of claim 22 wherein assigning comprises apportioning at least one DMA engine to process at least one transaction at a port.

25. (Previously presented) The method of claim 22 wherein assigning comprises apportioning one DMA engine to process a given transaction at a port identified as servicing multiple I/O devices.

26. (Previously presented) The method of claim 21 wherein assigning comprises assigning at least one miss address file (MAF) value for processing I/O transactions.

27. (Previously presented) The method of claim 21 wherein assigning comprises assigning a plurality of miss address file (MAF) values for processing I/O transactions.

28. (Previously presented) The method of claim 27 further comprising reducing the assigned number of MAF values.

29. (Previously presented) The method of claim 21 wherein

the I/O bridge is configured to utilize a plurality of virtual channels to communicate with at least one processors of a multiprocessor computer system, and

the resources include flow control credits associated with each of the plurality of virtual channels.

30. (Previously presented) The method of claim 29 wherein assigning comprises setting the number of flow control credits associated with each virtual channel.

31. (Previously presented) The method of claim 21 wherein

the I/O bridge comprises at least one control register, the at least one control register having a plurality of fields, and at least one field of the control register being associated with a corresponding resource, and

the method further comprises writing to a selected field of the at least one control register so as to modify the assignment of resources.

32. (Previously presented) An Input/Output (I/O) bridge for use in a computer system having a plurality of processors, the I/O bridge comprising:

a plurality of I/O ports, each I/O port configured to communicate with at least one I/O device that generates or receives transactions;

resources for use in servicing the transactions of the I/O devices; and

programmable logic configured and arranged to assign the resources among the I/O ports in response to the number of I/O devices with which the I/O ports are communicating.

33. (Previously presented) The I/O bridge of claim 32 wherein

the resources comprise at least one direct memory access (DMA) engine configured to process the transactions, and

the programmable logic apportions the at least one of DMA engine to process at least one transaction at a given I/O port in response to the number of I/O devices coupled to the given I/O port.

34. (Previously presented) The I/O bridge of claim 32 wherein

the resources include a plurality of miss address file (MAF) values for use in requesting information from the computer system, and

the programmable logic sets the number of available MAF values.

35. (Previously presented) The I/O bridge of claim 32 wherein

the I/O bridge communicates with the computer system through a plurality of virtual channels,

the resources include a plurality of flow control credits associated with the virtual channels, and

the programmable logic assigns a number of flow control credits to each virtual channel.

36. (Previously presented) the I/O bridge of claim 35 wherein the virtual channels comprise a Request channel, a Read I/O channel, and a Write I/O channel.

37. (Previously presented) The I/O bridge of claim 33 further comprising at least one cache for storing information, wherein, to hot-swap an assembly of the computer system, the programmable logic is configured to

disable the at least one DMA engine, and

flush the information from the at least one cache.

38. (Previously presented) The I/O bridge of claim 37 wherein the at least one cache is one of a write cache, a read cache and a translation look-aside buffer (TLB).

39. (Previously presented) The I/O bridge of claim 37 wherein the assembly is a processor.

40. (Previously presented) The I/O bridge of claim 33 wherein

the programmable logic comprises at least one control register associated with each I/O port, and

the at least one control register has a first field for apportioning the at least one DMA engine.

41. (Previously presented) The I/O bridge of claim 32 wherein the programmable logic re-assigns resources among the I/O ports dynamically while the I/O bridge continues to operate.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.